REMARKS

Claims 1-49 are pending. Claims 1, 17, 26, 33, 36, 42, and 46 are in independent form.

In the action mailed June 19, 2006, the Declaration was identified as defective for failing to identify the citizenship of inventor Greg Regnier.

Submitted herewith is a Substitute Declaration in accordance with M.P.E.P. § 602.02. Accordingly, the requirements of 35 U.S.C. § 115 are satisfied.

The Specification was objected to as including a title that is "not descriptive." Applicant respectfully disagrees. The independent claims clearly relate to translation of virtual addresses to physical addresses. For example, claim 1 recites "determining the physical address corresponding to the virtual address." Accordingly, the objection to the specification is respectfully traversed.

Claim 17 was objected to as being informal for reciting "the start of the virtual buffer." Applicant respectfully traverses the objection. In particular, it is self-evident that a virtual buffer has a start and thus antecedent basis for the start of the virtual buffer is based in the recitation of the virtual buffer itself. *See, e.g., M.P.E.P.* § 2173.05(e) (*citing Bose Corp. v. JBL, Inc.*, 274 F.3d 1354, 1359 (Fed. Cir. 2001)).

Claims 42 and 46 were objected to as including informal indenting. The indenting of claims 42 and 46 has been amended to address the Examiner's concerns.

Claims 8, 21, 38, and 40 were rejected under 35 U.S.C. § 112, second paragraph as indefinite on various grounds. These claims have been amended to address the Examiner's concerns.

CLAIM 1

Claim 1 was rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 6,360,282 to Langerman et al. (hereinafter "Langerman").

As amended, claim 1 relates to a machine-implemented method that includes receiving, by a first process in a first virtual memory address space, a shortcut to a physical address associated with a level of a multi-level virtual address translation table, posting a descriptor to an interface between the first process and a second process, and determining the physical address corresponding to the virtual address based on at least the virtual address and the shortcut. The descriptor comprises a virtual address in the first virtual memory address space and the shortcut. The second process is in a second virtual memory address space.

Langerman neither describes nor suggests posting a descriptor to an interface between the first process and a second process that are in different virtual memory address spaces, as recited in claim 1.

In this regard, Langerman's interface is a software interface that is presented to a user application for performing disk I/O. *See Langerman*, col. 4, line 8-10. Although Langerman's software interface supports multiple concurrent users (*See Langerman*, col. 4, line 14-20), Langerman does not establish an interface between those users. Indeed, one of Langerman's stated purposes is to prevent a user program from gaining unauthorized access to another user's registers. *See Langerman*, col. 4, line 21-24.

Accordingly, claim 1 is not anticipated by Langerman. Applicant requests that the rejections of claim 1 and the claims dependent therefrom be withdrawn.

CLAIM 17

Claim 17 was rejected under 35 U.S.C. § 102(b) as anticipated by Langerman. Claim 20 has been amended to recite subject matter drawn from claim 20, which was also rejected under 35 U.S.C. § 102(b) as anticipated by Langerman.

As amended, claim 17 relates to a machine-implemented method. The method includes generating, by a first process in a first virtual memory address space, a request to register a virtual buffer, identifying a block of memory that includes the physical address corresponding to the start of the virtual buffer, generating, by a second process, one or more shortcuts that map the block of memory that includes the physical address corresponding to the start of the virtual buffer, and transmitting a request to a third process in a second virtual memory address space to perform an input or output operation on the virtual buffer. The virtual buffer is in the first virtual memory address space and is mapped to physical memory by a multi-level virtual address translation table associated with the first process.

The rejection of former claim 20 contends that an individual user in Langerman is both a first process and a third process. Applicant respectfully disagrees, and submits that it is self-evident that a single user in Langerman cannot constitute two different processes (the first and third processes). Indeed, as discussed above, Langerman does not establish an interface between multiple users, but instead seeks to prevent a user program from gaining unauthorized access to another user's registers.

Since Langerman does not involve data transfer between multiple users, Langerman does not describe or suggest transmitting a request to a third process in a second virtual memory address space to perform an input or output operation on a virtual buffer in a first virtual memory address space, as recited in claim 17. Accordingly, claim 17 is not anticipated by Langerman. Applicant requests that the rejections of claim 17 and the claims dependent therefrom be withdrawn.

CLAIM 26

Claim 26 was rejected under 35 U.S.C. § 102(b) as anticipated by Langerman.

As amended, claim 26 relates to a system that includes a first processor and a second processor. The first processor is capable of executing instructions of a first process which causes the first processor to produce a shortcut to a physical address associated with a level of a multi-level virtual address translation table, and executing instructions of a second process in a first virtual memory address space which causes the first processor to post a descriptor comprising a virtual address and the shortcut to an interface. The second processor is capable of executing instructions of a third process in a second virtual memory address space which cause the second processor to read the descriptor posted on the interface, and determine a physical address of the virtual address based on at

least the virtual address and the shortcut. The interface is between the second process and the third process.

Langerman neither describes nor suggests such processors or such an interface. As discussed above, Langerman's interface is a software interface that is presented to a user application for performing disk I/O. Langerman does not establish an interface between users. Instead, one of Langerman's stated purposes is to prevent a user program from gaining unauthorized access to another user's registers.

Accordingly, claim 26 is not anticipated by Langerman. Applicant requests that the rejections of claim 26 and the claims dependent therefrom be withdrawn.

CLAIM 33

Claim 33 was rejected under 35 U.S.C. § 102(b) as anticipated by Langerman.

As amended, claim 33 relates to a computer program product residing on a computer readable medium having instructions stored thereon. When the instructions are executed by the processor, the instructions cause that processor to produce a shortcut to a physical address associated with a level of a multi-level virtual address translation table, and write a descriptor comprising a virtual address and the shortcut to an interface between a first process in a first virtual memory

address space and a second process in a second virtual memory address space.

Langerman neither describes nor suggests such a writing of a descriptor to an interface between a first process in a first virtual memory address space and a second process in a second virtual memory address space. As discussed above, Langerman's interface is a software interface that is presented to a user application for performing disk I/O. Langerman does not establish an interface between users. Instead, one of Langerman's stated purposes is to prevent a user program from gaining unauthorized access to another user's registers.

Accordingly, claim 33 is not anticipated by Langerman. Applicant requests that the rejections of claim 33 and the claims dependent therefrom be withdrawn.

CLAIM 36

Claim 36 was rejected under 35 U.S.C. § 102(b) as anticipated by Langerman.

As amended, claim 36 relates to a computer program product residing on a computer readable medium having instructions stored thereon. When the instructions are executed by a processor performing operations in a first virtual memory address space, the instructions cause that processor to read a message posted on an interface by a first process in a different virtual memory address space, determine a physical address of a

virtual address in the different virtual memory address space based on at least the virtual address and the shortcut, and transmit a message over a network based on contents of the physical address. The message includes a shortcut to a physical address associated with a level of a multi-level virtual address translation table.

Langerman neither describes nor suggests operations in a first virtual memory address space that include transmitting a message over a network based on contents of a physical address determined to be of a virtual address in a different virtual memory address space. As discussed above, Langerman's interface is a software interface that is presented to a user application for performing disk I/O. No message is transmitted over a network, much less a message based on contents of a physical address determined to be of a virtual address in a different virtual memory address space.

Accordingly, claim 36 is not anticipated by Langerman. Applicant requests that the rejections of claim 36 and the claims dependent therefrom be withdrawn.

CLAIM 42

Claim 42 was rejected under 35 U.S.C. § 102(b) as anticipated by Langerman.

As amended, claim 42 relates to a system that includes a client computer and a server in communication with the client computer using a network. The server includes a first processor and a second processor. The first processor is capable of producing a shortcut to a physical address associated with a level of a multi-level virtual address translation table and writing a descriptor comprising a virtual address in a first virtual memory address space and the shortcut to an interface. The second processor is capable of performing operations in a second virtual memory address space. The operations include reading the descriptor posted on the interface, determining a physical address of the virtual address based on at least the virtual address and the shortcut, and transferring data located at the physical address to the client computer using the network.

Langerman neither describes nor suggests a second processor that is capable of performing operations in a second virtual memory address space, including determining a physical address of a virtual address in a first virtual memory address space and transferring data located at the physical address to a client computer using a network.. As discussed above, Langerman's interface is a software interface that is presented to a user application for performing disk I/O. No data is transferred

data over a network, much less by a processor performing operations in a second virtual memory address space.

Accordingly, claim 42 is not anticipated by Langerman. Applicant requests that the rejections of claim 42 and the claims dependent therefrom be withdrawn.

CLAIM 46

Claim 46 was rejected under 35 U.S.C. § 102(b) as anticipated by Langerman.

As amended, claim 46 relates to a system that includes a storage device and a server in communication with the storage device over a network. The server includes a first processor and a second processor. The first processor is capable of producing a shortcut to a physical address associated with a level of a multi-level virtual address translation table and writing a descriptor comprising a virtual address in a first virtual memory address space and the shortcut to an interface. The second processor is capable of performing operations in a second virtual memory address space. The operations include reading the descriptor posted on the interface, determining a physical address of the virtual address based on at least the virtual address and the shortcut, and transferring data located at the physical address to the storage device using the network.

Langerman neither describes nor suggests a second processor that is capable of performing operations in a second virtual memory address space, including determining a physical address of a virtual address in a first virtual memory address space and transferring data located at the physical address to a storage device using a network.. As discussed above, Langerman's interface is a software interface that is presented to a user application for performing disk I/O. No data is transferred data over a network, much less by a processor performing operations in a second virtual memory address space.

Accordingly, claim 46 is not anticipated by Langerman. Applicant requests that the rejections of claim 46 and the claims dependent therefrom be withdrawn.

Applicant asks that all claims be allowed. No fees are believed due at this time. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: August 21, 2006

Scott C. Harris
Reg. No. 32,030

Fish & Richardson P.C.
PTO Customer No. 20985
12390 El Camino Real
San Diego, California 92130
(858) 678-5070 telephone
(858) 678-5099 facsimile

SCH/JFC/jhg
10655643.doc